ABSTRACT OF THE DISCLOSURE

The first model described in a software description language is converted into the second model described in a hardware description language without considering whether a plurality of parallel procedures for writing with respect to the same shared variable are contained in the first model. It is detected whether a plurality of parallel processes corresponding to the plurality of parallel procedures for writing with respect to the same shared variable exist in the second model obtained in this manner. A value solving process is generated, in which a pair of a data signal and an assignment timing signal are input from each process of all or some of the detected parallel processes, and a signal of the data signals which corresponds to a process in which the assignment timing signal has changed is output to a signal holding the value of the shared variable.